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SEMICONDUCTOR TEST CONSORTIUM EXPANDS SCOPE TO ENCOMPASS THE ENTIRE TEST PROCESS

NIWOT, Colorado, October 23, 2006 — The Semiconductor Test Consortium, Inc. (STC), the leading proponent of worldwide adoption of Open Architecture, today announced an expansion in scope through a new initiative to enable development of automatic test equipment (ATE) peripheral interface standards. This new initiative will treat the ATE as a “black box”, enabling greater portability of test collateral through higher level abstraction of user programming, equipment integration, and device interconnect. The Docking and Interface Working Group (DIWG) has been created and joins the existing STIL and Probecard Working Groups as a first step of this expansion. Additional working groups are forming to focus on definition of a User-Level Application Programming Interface (API), Instrument Portability/Abstraction Layer, Tooling (device interface) Abstraction Layer and Asynchronous Device Test Interface. These newest working groups will enable the STC’s work to encompass more of the entire test process—delivering further benefits for the global semiconductor industry.

“As a direct result of feedback from STC members and the industry as a whole, we have chosen to expand the consortium to encompass the entire test process. In addition to validating the STC’s commitment to listen to members and industry thought leaders, today’s announcement demonstrates that we are taking proactive steps to meet these industry needs,” stated Don Edenfeld, STC Chairman. “This is just the beginning of a significant shift in the focus of the STC, as there is much work ahead for the organization to bring this expansion to fruition with full implementation planned by the end of the year.”

The DIWG will concentrate on development of technical definitions and specifications for docking and interfacing of peripheral test equipment, such as wafer probers and device handlers, with ATE. This working group addresses a critical industry need for standardization that will provide substantial economic and technical benefits to users and vendors alike. The initial DIWG roster includes members from Reid-Ashman Manufacturing, Inc., Microhandling GmbH, Intel Corporation, Infineon Technologies AG, Esmo AG, Analog Devices, Inc. and Advantest Corporation.

The STC will continue to enable the OPENSTAR[®] Ecosystem through continuous improvement of the existing set of specifications and member driven focused efforts. In addition, the newly formed OPENSTAR Solutions Working Group (OSWG) will define and execute a process for collecting test requirements and solutions from STC members, which will in turn produce an end-user’s “Test Requirements Roadmap” and a vendor’s “Products Roadmap.” These roadmaps may encompass many requirements from the ecosystem, including, but not limited to, test instrument modules, test systems, interfaces, software tools, support services, etc. The financial and infrastructure benefits these products provide STC members are critical to ensuring success in today’s dynamic consumer-driven semiconductor market.

“These new working groups are yet another strong indication that the STC continues to mature and expand in various segments within and around ATE that will benefit the entire semiconductor industry,” stated Bob Helsel, STC Manager and Secretary. “In Phase I, the consortium was successfully launched, OPENSTAR hardware and software specifications were developed and published and STC reached a critical mass of members. In Phase II, the STC gained industry traction, the first third party modules were developed and deployed, and the specifications were improved. Phase III goals center on expanding the STC’s scope to encompass the entire test process outside of ATE. Based on the feedback from members and non-member participants at the Global STC Conference in March and in the many worldwide meetings, there is a great demand for additional working groups such as the DIWG to focus on providing technical and economic benefits to the industry.”

The STC will exhibit at the International Test Conference (ITC), October 24-26, 2006, in Santa Clara, Calif., in booth #113. Additionally, it will hold a University Working Group meeting from 2:00-5:00 p.m. on October 23 at Advantest America, 3201 Scott Blvd., Santa Clara, Calif. The next STC general meeting is scheduled for November 29 and 30 in

Phoenix, AZ.

About the Semiconductor Test Consortium

The Semiconductor Test Consortium was founded in 2003 to develop a common test architecture that is completely open, documented and supported via solutions available from all ATE vendors. Open to all companies throughout the semiconductor supply chain with a vested interest in the test sector, the consortium is focused on the following goals: formalizing a broadened STC scope with new working groups and specification structure; fostering pre-competitive collaboration among industry participants toward development of value-added standards; emphasizing new initiatives, the value of work being accomplished and the contributions to the industry; and continuing STC efforts to fully enable the OPENSTAR Ecosystem. Today, 44 semiconductor, equipment and instrumentation companies worldwide and 36 universities in Europe, Japan, China and the United States, in addition to eight STIL users and three individuals support the STC. More information can be found at www.semitest.org

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