Benefits Of A True 'Open Architecture Tester' Model

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Semiconductor manufacturers are driving a new paradigm shift in semiconductor testing! Fed up with trying to efficiently manage test floors filled with a variety of tester models from multiple vendors, semiconductor manufacturers have started an initiative to drive development of an "open architecture tester" model. Although somewhat reluctant, the tester equipment vendors are responding to this user effort.

According to recent press releases, almost all of the major test equipment vendors have announced their own open architecture tester initiatives. In reality, most appear to be continuing their previous model of "proprietary" tester designs, although allowing some limited, non-competitive, third-party module designs.

Current State Of The Industry

The semiconductor industry is still struggling to recover from the worst downturn in history. Tester vendors are having a difficult time maintaining previous R&D funding levels. DFT (scan and BIST) and structural test techniques are eliminating the need for at-speed testing and are enabling a migration to lower cost testers. Semiconductor manufactures are continuing to aggressively drive down their cost of test. This is not a very rosy picture for the already crowded test equipment market.

Today's proprietary tester model has not served the industry well. There is probably not a single tester company that can provide complete and efficient test coverage for one of today's large semiconductor company's diverse test needs. Test floors of semiconductor companies are filled with testers from multiple companies. Many inefficiencies result from this variety of testers. During the recent industry downturn, companies were adding additional tester capacity of one type, while other testers were sitting idle, due to difficulty in migrating from one tester platform to another.

Migration of testing from one platform to another is a difficult and time-consuming process. Because of the difficulty, companies tend to stay on test platforms beyond their prime. Maintaining multiple tester platforms is costly. All of these issues are driving the need for standardization in the test arena. The concept of a standard tester language was introduced and effort was started on the IEEE STIL specification. Adoption of the STIL standard has been minimal. Semiconductor manufacturers, fed up with the array of testers that were required to cover their test needs, started the open architecture tester model initiative.

What Is A True Open Architecture Tester?

In today's terms, "open architecture" is generally recognized to be an architecture whose specs are open to the public, allowing unlimited and unrestricted third-party development.

For the semiconductor test environment, "open architecture tester" is a phrase coined by the Semiconductor Test Consortium to describe a tester with specs open to the public to allow any company to develop hardware (modules or complete test systems) and software (modules or complete operating systems). Only one of the major tester vendors has adopted this true open architecture tester model.

The open architecture tester is expected to provide test capability for all types of semiconductor products. The open architecture tester mainframe and test head design is expected to last eight to 10 years, with new test capability added via new module designs, not a complete tester redesign. Table 1 outlines some of the basic differences between today's proprietary architecture tester model and the open architecture tester model.

Benefits Of Open Architecture Tester

A true open architecture tester model will provide many benefits to both the test equipment users and test equipment vendors. Contrary to popular belief, the semiconductor manufacturers are not just trying to drive down the capital equipment costs.

Actually, the cost of integrating very-low-cost testing into the open architecture tester model may actually increase the capital cost of this low-cost equipment, but this increase will be offset by the many other benefits such as standardization and direct competition.

Standardization

The biggest benefit that the open architecture tester model provides to semiconductor manufactures is standardization. The open architecture tester will provide a common test software language as well as a common hardware/software interface between the tester and handler/probers.

Granted, migration to an open architecture tester will be the same effort as moving to any other tester, but the big benefit will be one to two years down the line when new test capability is needed. Adding new test capability to the open architecture tester will only require adding a new module. This standardization will substantially reduce the effort and time required to add new test capabilities. Engineers will not be required to learn a

Today's Proprietary Architecture	Open Architecture
One or more proprietary architectures for each tester vendor	Common architecture shared by multiple vendors
Single source for tester and parts	Multiple sources for testers and parts
Proprietary programming languages	Common programming language across multiple vendors
Proprietary hardware I/F to handlers and probers	Common hardware I/F across tester vendors
Custom porting of third-party software tools to tester	Software is written once and applies to all "open architecture testers"
Major effort to migrate to other vendor's tester	No to minimal migration effort

Table 1. "Open" Vs. "Proprietary" Tester Model

new programming language and take a year or two to become proficient in a new tester language. New test vector/program generation tools will not have to be written or acquired to support new testers. Adding new test capability via new modules will almost be invisible to the test floor, requiring minimal support. Equipment maintenance costs will be substantially reduced with a common open architecture tester, with reduction in cost of spare boards and maintenance training.

Direct Competition

The open architecture tester model will provide direct competition between vendors. Semiconductor manufacturers will have a choice of whom to purchase mainframes, modules or software tools from. This direct competition will result in lower purchase costs, faster time to market, improved delivery and better technology (a vendor will want to provide better features such as accuracy or reliability to differentiate its products from the competition).

Lower Barrier For New Technology

The open architecture tester will lower the barrier for migration to new or next-generation technologies. With today's proprietary tester model, a new tester has to have substantially better – 30 to 40 percent better – cost-of-test to enable the costly and time-consuming migration to the new tester platform. The open architecture tester model of just adding a new module will enable quicker migration to new technologies. With open architecture, companies can take advantage of new technologies that provide only 5 to 10 percent better cost of test.

The open architecture tester will also provide a lower barrier for new tester companies entering the market. A new company need not be able to design a complete test system. A company can just build a new power supply or develop a new shmoo software tool.

Obsolescence Proofing

The open architecture tester model will provide protection from obsolescence. In today's time, when a vendor decides not to provide future enhancements to a tester architecture, there is no other solution to expand the tester. In the open architecture tester model, it is expected that there will be multiple third-party vendors willing to design new enhancements to extend the life of the tester. The open architecture tester model will reduce dependence on a single vendor to provide needed enhancements.

Tester Vendor Benefits

A true open architecture tester model will also provide benefits to the test equipment vendors. Adoption of a common open architecture tester model will reduce the test equipment industry's redundant R&D effort and will allow the industry to focus on key module technology. The cost of developing and maintaining new mainframes, testheads and tester operating system software will be substantially reduced.

When test software tool vendors develop a tool, they have to port it to multiple vendors testers. With the open architecture tester model they can develop a tool and work on providing enhancements instead of porting it to various other tester platforms.

Use of the open architecture tester standards will greatly reduce the amount of time and effort required to bring up a new customer's product, enabling a faster time to test equipment sales.

The open architecture tester model will provide a bigger market for test equipment vendor's products. Today a vendor's modules will fit only their proprietary tester. In the open architecture tester model, a vendor's module can potentially fit into any tester that adheres to the open architecture specs.

Associated Risks

As with any new technology, there are risks associated with the open architecture tester model. Most semiconductor manufacturers agree on the need for a standard open architecture tester, although some doubt that the model will work for VLSI-level testing. Can multiple vendors build modules and have them work in a common architecture? What happens if every vendor declares their architecture to be the industry standard? Does the open architecture tester model present a viable business model for test equipment vendors?

Summary

A true open architecture tester model provides some overwhelming benefits that cannot be ignored. The fact that almost ever major tester vendor has announced their own open architecture tester lends strong credibility to this initiative. Hopefully, test equipment vendors will respond to this user-driven initiative and adopt the true open architecture model. Will the industry evolve to a single open architecture tester model? Probably not, but compared to today's 40 to 50 tester models, the effort could be considered a tremendous success if two or three standard tester architectures evolve. ■

Biography

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Paul Roddy is the ATE technology manager of Freescale Semiconductor (www.freescale.com) and is also the chairman of the board for the Semiconductor Test Consortium (www.semitest.org). He is a 29-year veteran of the semiconductor test industry, having worked in chip, board and system level testing in the IDM and subcon environment. He can be contacted at Paul.Roddy@freescale.com.